High Gain and Frequency Ultra-Stable Integrators

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Abstract:
Eagle Harbor Technologies has received DOE Phase I SBIR funding to continue the development of high gain and stability integrators that are capable of high bandwidth measurements over long pulse operation. The present design operates with a 10 us RC time, for pulse durations up to the second time scale, with a frequency response in excess of 10 MHz, and typical drift errors of under 10 mV. This integrator development consists of two primary tasks. The first is to demonstrate stable operation over the much longer time scales required by ITER. When a proper comparison between available integrator designs is made that normalizes for gain and operation time, the existing integrators are the best available and meet ITER requirements for stability. However, this stability needs to be demonstrated over the hour type time scales relevant to ITER, as opposed to the very high gain second type operation typically used within the ICC community. The second primary task is to incorporate the integrators into the National Instruments (NI) platform to allow for easy operation with modern DAQ systems.

Comparison with Other Integrators:

The table shows a list of the most developed long pulse integrators systems, mostly as specified by Vayakis and Walker, along with a comparison to the RPPL integrator. For ease of comparison due to the different testing conditions and operational durations, a figure of merit has been developed for each integrator system, which accurately reflects the integrator drift as a function of RC time and operational duration. The figure of merit is simply the drift error normalized to the integrator's operational time. Though many papers simply compare integrators by stating a run time and the drift error, which is the absolute drift during the run time multiplied by the integrator's RC time constant, the figure of merit is presented since the RPPL integrators have been operated under such different conditions. Specifically, they have been operated with a gain that is about four orders of magnitude greater than those integrators specifically developed for long pulse operation. Thus the duration of operation is correspondingly shorter. It is clear that most integrators perform much better under bench test conditions than under actual experimental conditions. The RPPL integrators are the exception. The primary reason for this likely has to do with them being used on the TCSU experiment in a properly shielded environment provided with isolated power, while when they were being bench tested, minimal effort was made to shield them from the generally noisy lab environment.

Integrator Type	Test Conditions	Duration (sec)	Drift Error (V sec)	Fig of Merit (V sec/sec)
ITER Target [9,10]	In Situ	> 1000	$< 2\times10^{-3}$	$< 2\times10^{-6}$
Analog dig. comp. (JET)[11]	Office Desk	25000	5×10^{-3}	2×10^{-7}
Volt to Freq conv. (JAERI)[12]	Bench	200	2×10^{-5}	1×10^{-7}
	Tokamak	2000	1×10^{-2}	5×10^{-6}
Hybrid dig/analog (DIII-D)[13]	Bench	1200	1×10^{-3}	8×10^{-7}
	Tokamak	1200	5×10^{-3}	4×10^{-6}
Dual comp. analog (Tore Supra)[14]	Tokamak	1000	1.35×10^{-4}	1.4×10^{-7}
RPPL analog integrators (TCSU)	Bench	1	5×10^{-8}	5×10^{-8}
	RMF FRC	1	5×10^{-8}	5×10^{-8}

The key take away message from table is just how well the RPPL integrators compare. Under actual experimental conditions, the RPPL integrators have a figure of merit that is about three times better than the next best integrators, those made by Tore Supra. The Tore Supra integrators have been referenced as the gold standard of long pulse integrators. If the performance of the RPPL integrators holds up under long pulse operation, not only will they become the best available, but they will have the additional benefit of being able to operate at much higher frequencies. For example, the Tore Supra integrators have a slew rate of ~ 0.2 V/µs while the RPPL integrators have a slew rate in excess of 10 V/µs. This means that with the change of the integrator's RC time constant, the RPPL integrators would be useful to both very fast high resolution applications, as well as long pulse applications. It is this versatility that makes them of interest to both the ICC community and the long pulse tokamak community.

* Recently ITER has raised it's target value for Figure of Merit to 7x10^-8

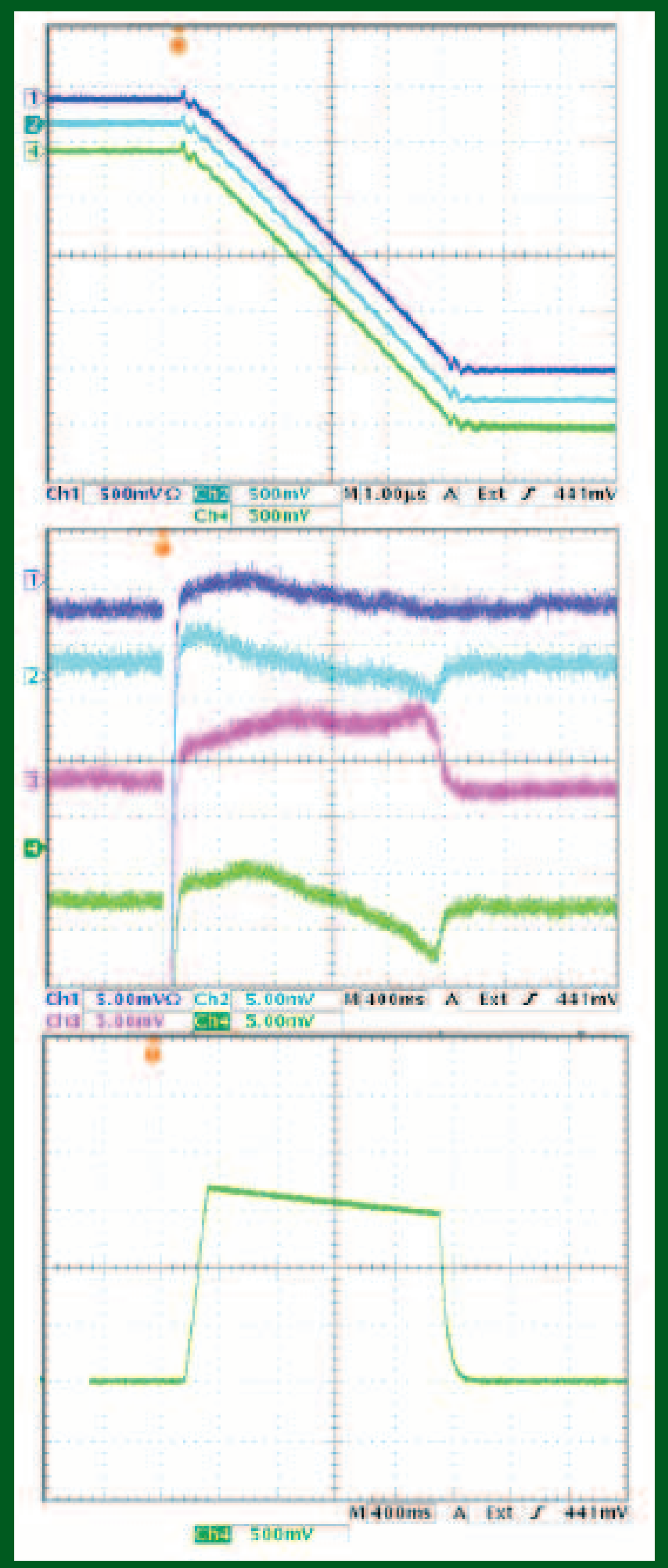
Integrator Program Objectives:

1. Optimize existing integrators and product low cost option for fusion science and laboratory applications.
   A) Several second operational time.
   B) Rack mount unit with variable connector options.

2. Configure integrators for long pulse applications > 1000 seconds. (ITER)
   A) Maintain Figure of Merit over long durations.
   B) Reduce or eliminate droop over long durations.

3. Incorporate integrator system into widely use DAQ modules for ease of use.
   A) National Instruments, PXI integration with software control

Integrator Output:



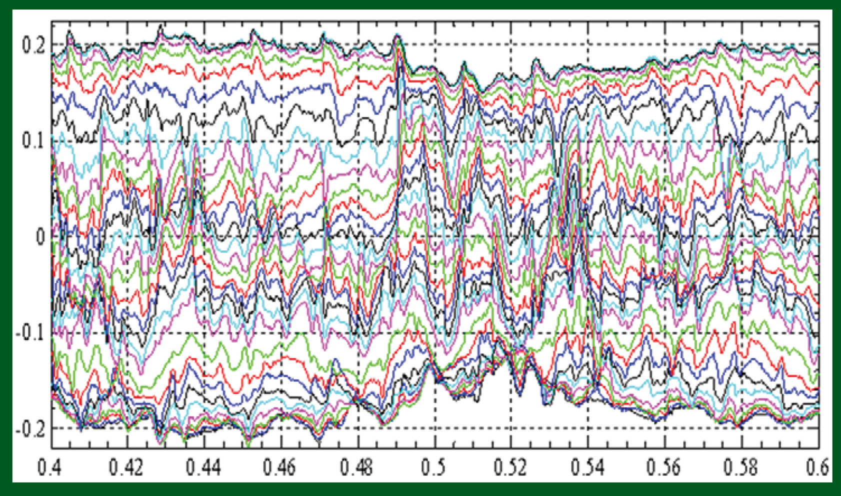
The EHT integrators are based on a fairly standard design for analog differential integrators, but the design utilizes very careful component selection, circuit board design and optical isolation for control signals.

The basic integrator board consists of 4 channels of differential operation amplifier with a sample and hold feedback circuit. Optically isolated gating is employed to eliminate ground loop type feedback, and the output buffer allows a wide range of output options to be driven, including 50 Ω.

The top traces show the integrator response to an input 8 V square pulse lasting for a period of 4.6 µs (3 of 4 channels shown).

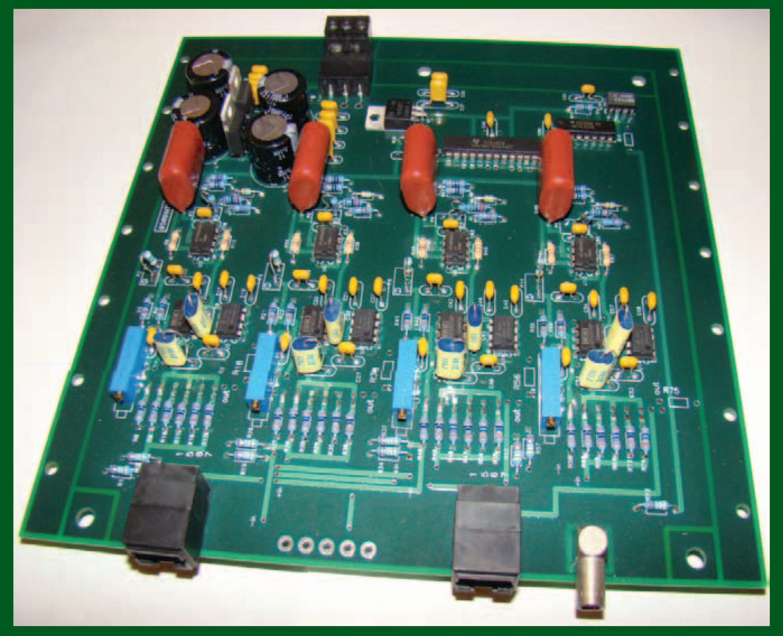
The middle trace shows the long term stability, with the integrators typically drifting around 5 mV during the 2 s period they are gated on for (4 of 4 channels shown). The initial negative spike seen in the data can be ignored.

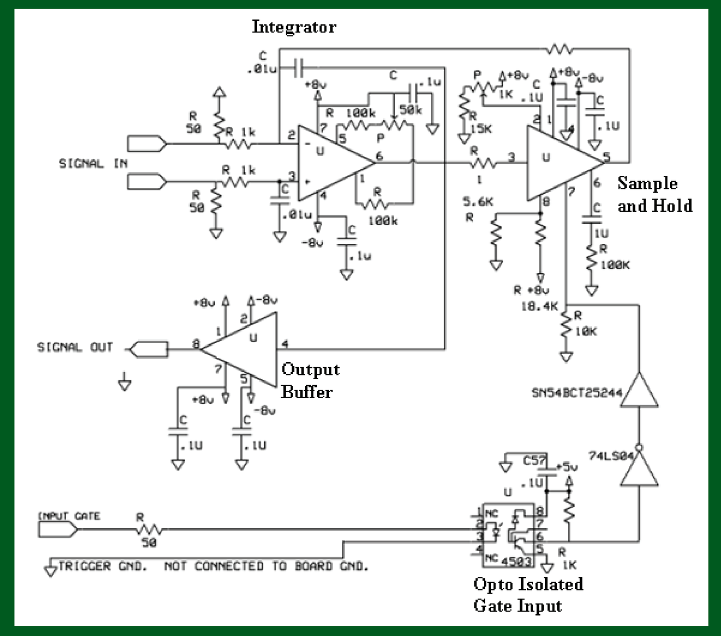
The bottom trace shows the ability of the integrators to hold a steady output voltage after an initial rapid integration. The droop shown in this trace is likely the result of the finite open loop gain of the actual op-amp used. Different higher gain op-amps are under study to address this issue (1 of 4 channels shown).



Magnetic field (kG) vs time (ms) for a typical TCS plasma (axial field component). Each trace corresponds to a probe at a different radial location, where the uppermost trace was at the edge of the plasma, and the lower most trace was the center of the plasma.

Pre-Phase I Design:

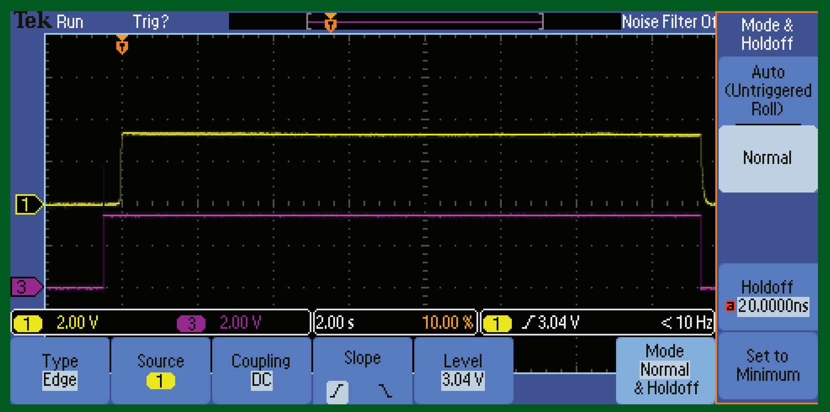




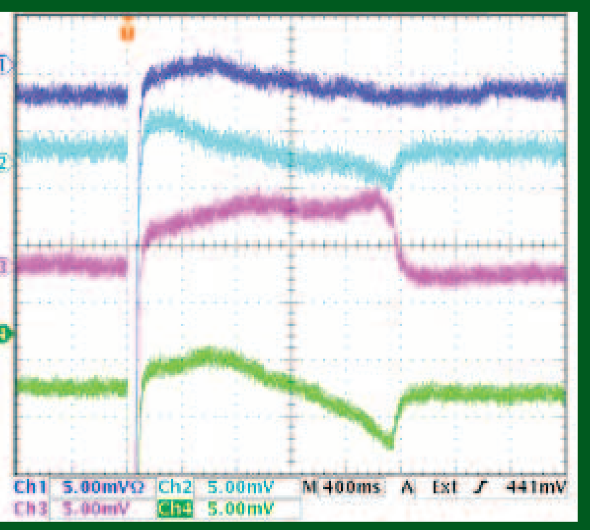
Pre-Phase I, High gain integrator board and circuit diagram. The simple design provides a low cost option for the integrators with performance realized through careful board design and component selection. The pre-Phase I design is suitable for applications requiring integration times for several seconds. The Phase I program will incorporate new features to dramatically reduce droop and overall drift over much longer periods appropriate for long pulse applications

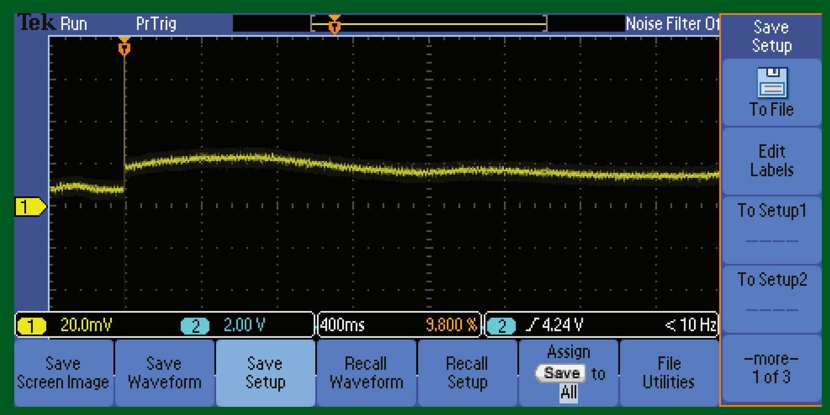
Phase I Progress:

The Phase I progress to date is focused on SPICE modeling, new architecture and board design to increase performance of the integrators to meet the current ITER specifications. Several new configurations have been tested with significant improvement in droop reduction of the integration system which maintaining similar drift. Concepts for drift reduction over long duration are now being investigated.



Pre-Phase I program integrator droop measurement (Left). Integrator output for the Phase I design showing little droop over 10s of seconds (Right).





Pre-Phase I program integrator drift measurement (Left). Integrator output for the Phase I design showing similar drift over a longer time period (Right). New methods for drift reduction are currently under investigation.

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