Solid-State Klystron Driver for Lower Hybrid Current Drive (Phase I)

J.R. Prager*; T. M. Ziemba; K. E. Miller; A. Henson
*prager@eagleharbortech.com

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Introduction

Launching radio frequency (RF) waves from the high-field side (HFS) of a tokamak has the potential to be an efficient off-axis current drive method while reducing the plasma-material interaction issues of the antenna. Researchers at the Plasma Science and Fusion Center (PSFC) at the Massachusetts Institute of Technology (MIT) have proposed to reuse existing equipment at MIT, including CPI klystrons, to demonstrate HFS RF launching at DIII-D. Eagle Harbor Technologies (EHT), Inc. is developing the next-generation klystron driver for use by MIT for HFS RF launching experiments at DIII-D. The next-generation klystron driver will take advantage of the high frequency solid-state switching capabilities developed by EHT with support of the DOE SBIR program. The high frequency nature will allow for the development of a more compact system, which can be placed closer to the klystrons. This system will be designed so that there is one driver per klystron, which will allow the system to scale as more klystrons are added and experiments to continue in the event of a klystron fault. We will present the Phase I project plan and overview of progress to date.

Current Klystron Driver

The MIT CPI klystrons were driven with a high voltage power supply (HVPS) that produced 50 kV pulses for up to five seconds and drove up to eight klystrons in parallel. Fault mitigation is an important issue for klystron drivers. The power system must rapidly remove voltage without dumping significant energy into the klystron in the event of a beam fault. The system was large, about the size of two shipping containers stacked. It must be located far from the klystrons, which means that there is significant cable length. In the event of a fault, there is significant energy that is stored in the cable inductance. Even if the power system stops, the energy stored in this inductance would likely be dissipated into the klystron and exceed the safe limits for energy deposited into the klystron. In the current klystron HVPS, all the klystrons are connected in parallel from a single supply. If a single klystron faults, all the klystrons are shut down.

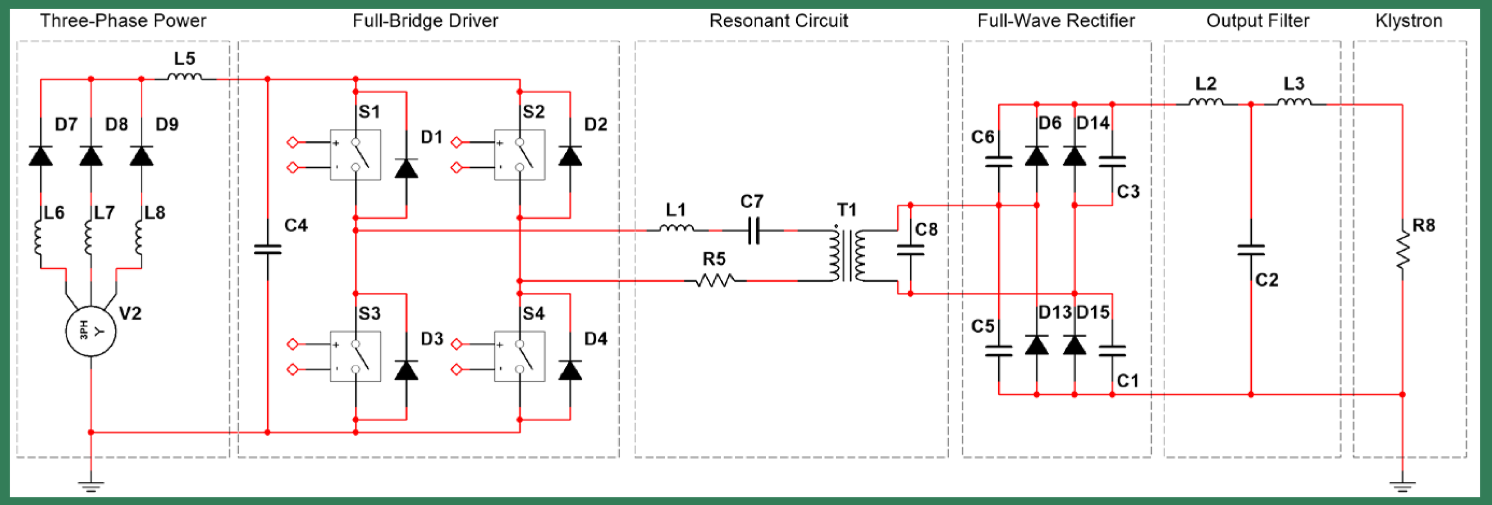
Next-generation Klystron Driver Requirements

The next generation klystron drive should have the following specifications to meet the requirements of operating the MIT CPI klystrons at DIII-D:

- Output voltage: 50 kV
- Output current: 12 A/klystron
- Rise time: 600 µs (faster is better)
- Fall time: 30 µs
- Pulse length: 10 s every 10 min
- Fault protection built in
- Input from three-phase power (13.8 kV in MA and 12.5 kV in CA)
- Compact design located in close proximity to klystrons

Circuit Modeling

A series-resonant converter with fast response times could be developed to produce the next-generation klystron driver. This system would convert rectified three-phase power to produce the 50 kV/12 A pulse needed to drive the klystron.



Simplified Multisim circuit model. Actual circuit model included stray components.

Single Device Testing

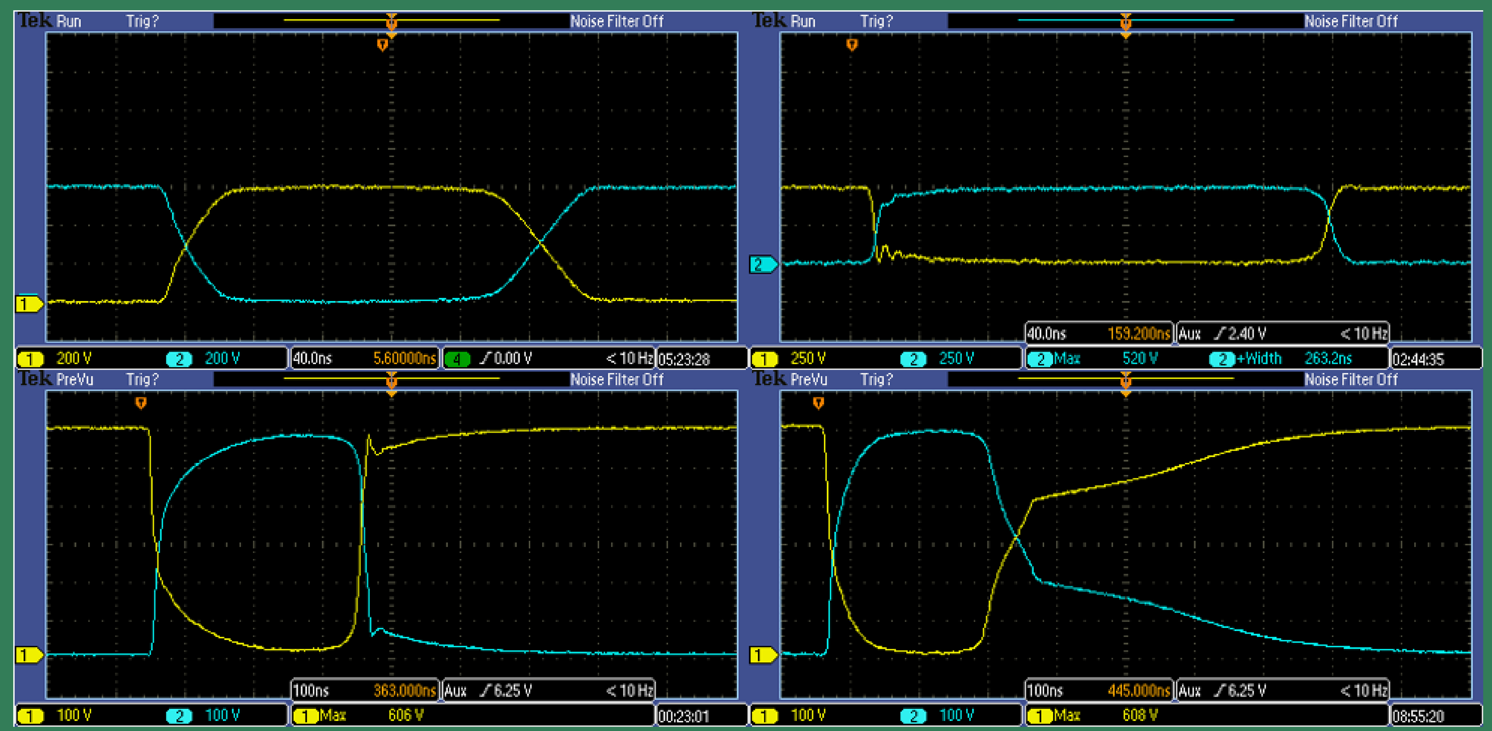
This testing was to determine the best suited switch for operation in the klystron topology. EHT evaluates switch rise and fall times into resistive loads, high-frequency robustness, and short-circuit capability. Our standard IGBT does not contain a body diode, so this test was used to compare devices with body diodes to our standard switch.

- Standard IGBT is black
- APT25GR120BD15 (75A) is blue
- FGH12040WD-F155 (40A) is red
- STGWA40N120KD (80A) is green

# of Pulses \ Frequency	200 k	500 k	1 M	2 M
1 k	✓✓✓✓	✓✓✓	✓✓✓	✓✓
2 k	✓✓✓✓	✓✓✓	✓✓✓	✓✓
5 k	✓✓✓✗	✓✓✓	✓✓✓	✓✓
10 k	✓	✓✓✓	✓✓✗	✓✓
20 k			✓✓	✓✓
50 k				✓✓
100 k				

# of Pulses \ Frequency	200 k	500 k	1 M	2 M
1 k	✓✓✓✗	✓✓	✓✓	✓✓
2 k	✓✓✗	✓✓	✓✓	✓✓
5 k	✓✓	✓✓	✓✓	✓✓
10 k		✓✓	✓✓	✓✗
20 k			✓✓	✓
50 k				✗
100 k				

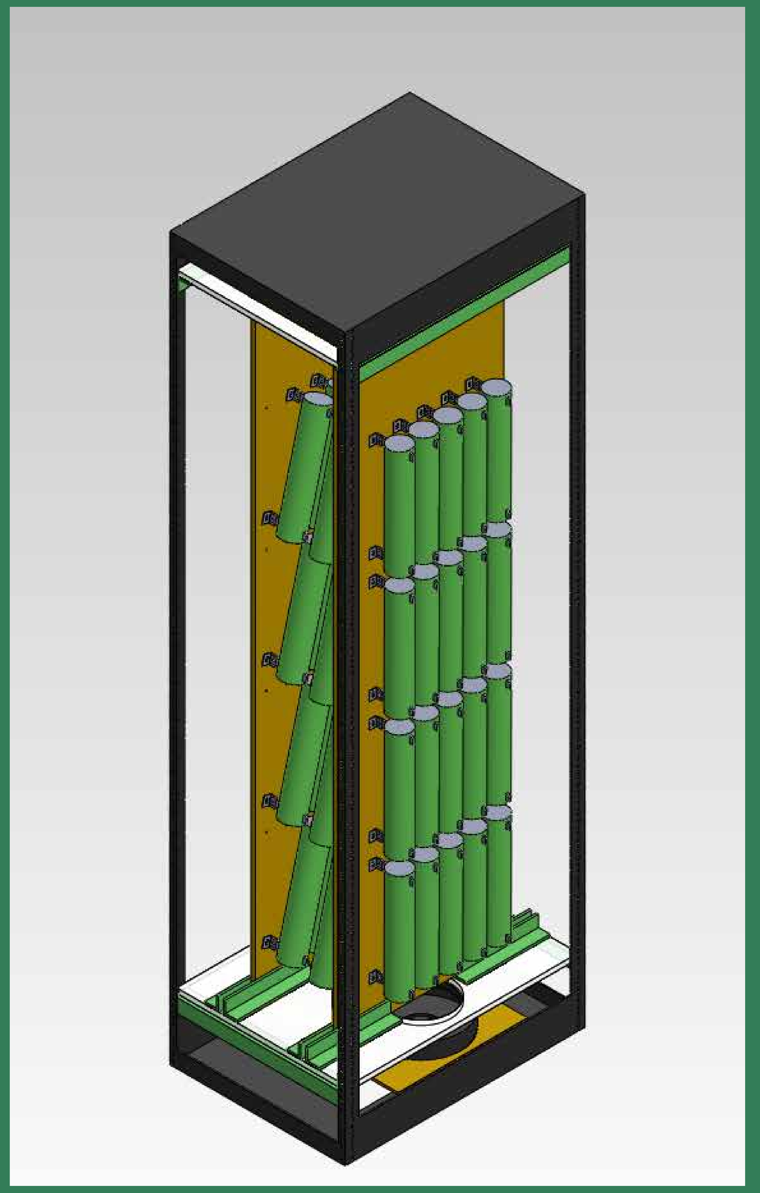
Parameter space of device testing for 30 A (top) and 80 A (bottom). Check means device passed; X means device failed.



Switching waveforms at 600 V and 20 A with 10 Ω gate resistor. Top left: Standard. Top Right: APT25GR120BD15. Bottom Left: FGH12040WD-F155. Bottom Right: STGWA40N120KD.

Klystron Driver Design

To drive a single klystron, 600 kW is required; however, the EHT facility does not have 600 kW available. In the Phase I, EHT is developing a pulsed power supply capable of switching 150 kW peak, 30 kW average power. EHT has begun developing a test load that can be operated at 30 kW continuously. This system can then be operated at 150 kW at MIT or DIII-D. In order to drive a single klystron, four of these modules operating in parallel will be required.



30 kW load resistor CAD model.

Conclusion

EHT's Phase I SBIR is under way to develop the next-generation klystron drive for testing HFS RF launching at DIII-D. EHT's design relies on the state-of-the-art solid-state switching to build a more compact robust klystron driver that can easily be scaled to multiple klystrons. EHT has conducted intial SPICE modeling to identify areas of concern that must be addressed as well as to validate the overal system design. EHT has selected switches and will begin integrating them into a previously designed full-bridge configuration. This system will be tested into a resistive load at 30 kW average power and 150 kW peak power.

In a potential Phase II program, EHT will continue the development of the next-generation klystron driver. The goals will be to operate multiple full-bridges in parallel, test faults conditions, and integrate a controller. Finally, EHT would test a single klystron driver at MIT with the CPI klystrons. At the end of a potential Phase II program, EHT would have a klystron driver design that could be commercialized.

For more information: http://www.eagleharbortech.com/

Acknowledgment

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