The Road to Short Pulses at 50 kV: Inductive Adder for High-Energy Beam Kickers

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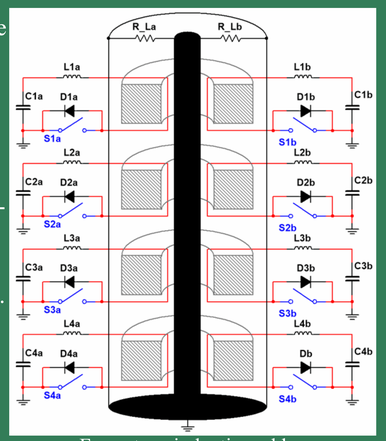
EAGLE HARBOR TECHNOLOGIES

Introduction

The 150 MeV energy recovery LINAC for the Electron Ion Collider being developed by and constructed at Brookhaven National Laboratory (BNL) requires a short-pulse stripline kicker. The kicker power system must deliver ±50 kV pulses with pulse widths of less than 38 ns into a 50 Ω load and with low jitter. The kicker power system must be highly reliable and robust to potential faults. To address this need, Eagle Harbor Technologies is developing a 50 kV inductive adder that can meet the challenging pulse requirements of BNL. In the Phase I, EHT designed a single inductive adder stage to demonstrate the pulse characteristics including fast rise and fall times, low jitter, and flat-top stability while operating at the full current, 1 kA. In Year 2 of the Phase II program, EHT has designed the transformer for the inductive adder and updated the printed circuit board design. EHT will present the development status and output waveforms.

Inductive Adder

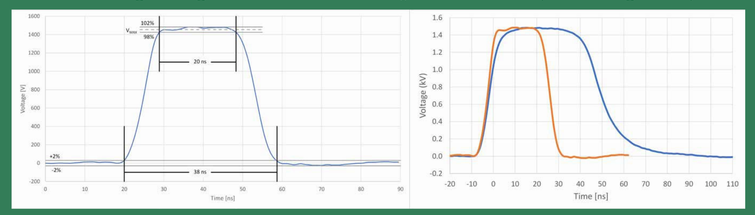
- Limits the presence of high voltage to the transformer.
- Ground-referenced switches increases robustness, simplifies gate drive design, and reduces jitter.
- Solid-state switches allow for user-adjustable pulse widths.
- Off-the-shelf components are used within manufacturer specifications.
- Single stage failure does not fail the entire power system.
- The output can be modulated to improve the flattop with the addition of a modulation stage.



Four-stage inductive adder.

Phase I Single-Stage Results

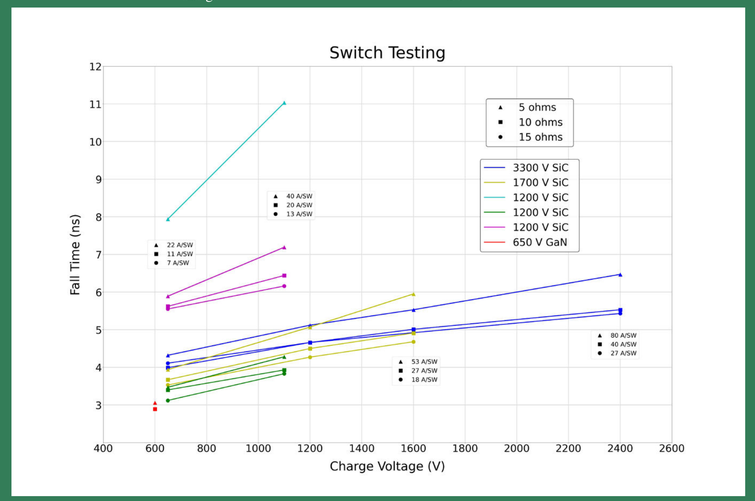
- Changed switch from IGBT (D^{3}PAK) to SiC MOSFET (TO-263-7)
- Added tailbiter switches to reduce the pulse fall time
- Changed layout from octagonal to circular switch arrangement
- Minimized stray inductance and capacitance of PCB
- Tested single stage board into 50-Ω equivalent load (switching 1 kA)



Left: Single-stage output voltage meets BNL requirements while switching 1 kA..
Right: Comparison of this work (orange) with the previous PCB design (blue).

Solid-State Switch Testing from Unrelated EHT Program

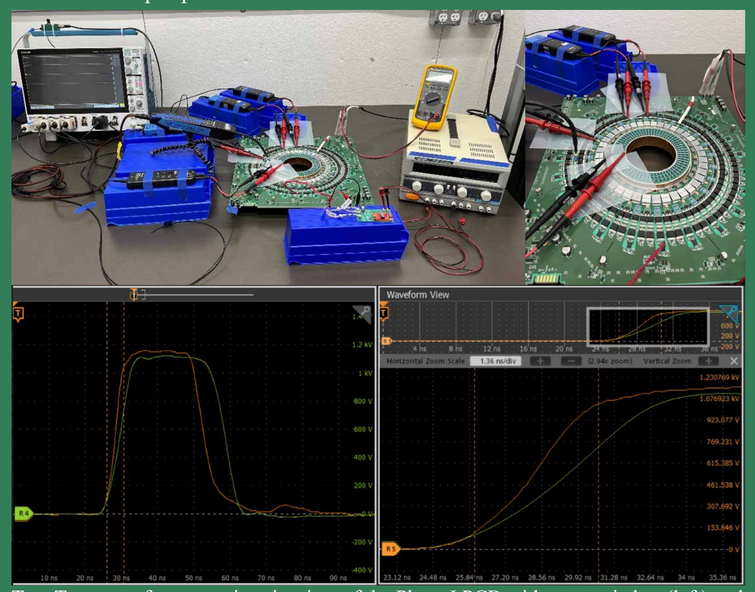
- V_{DS} fall times are much faster datasheets suggest.
- V_{DS} fall times typically increase as the current per switch increases.
- Increasing the V_{charge} does not increase the V_{DS} fall time by the same factor.



V_{DS} fall time as a function of V_{charge} and current per switch for GaN and SiC devices.

New Switch Testing with Phase I PCB

- New SiC MOSFETs have faster transitions at higher current per switch while reducing system cost.
- Reduced output pulse rise time from 6.4 ns to 4.7 ns.



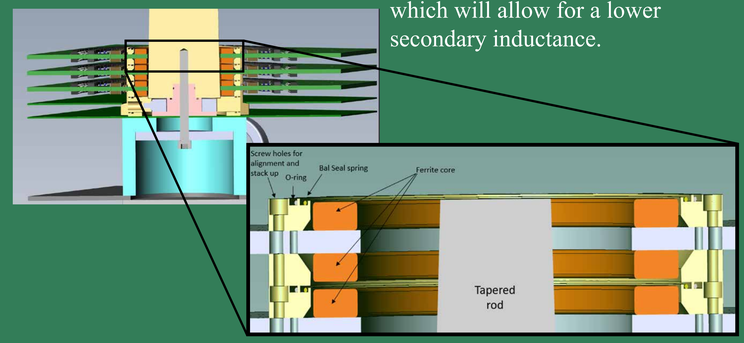
Top: Test setup for measuring rise time of the Phase I PCB with new switches (left) and closeup showing probe locations (right). Bottom: Output waveform with new (orange) and old (green) switches on two different timescales.

Evolution of Inductive Adder PCB

Comparison of EHT inductive adder PCBs: original design (left), Phase I design (middle), Phase II design with new SiC MOSFETs.

Mechanical Design of Inductive Adder Transformer

The transformer will be filled with SF_6 to help minimize standoff required, which will allow for a lower secondary inductance.



Top: Bottom three switching boards of the inductive adder stack. The central transformer rod is in yellow. Bottom: Closeup showing transformer ring design. Note that the bottom figure is from a different location in the stack.

Conclusion

EHT is developing an inductive adder to drive the stripline kickers at BNL EIC that will produce 50 kV pulses with fast rise (< 6 ns) and fall times (<12 ns) with a flat top ripple below 2%. EHT has identified new SiC MOSFETs that improve the output pulse rise time and operate at higher current per switch. These switches allowed for a new PCB design and a significant reduction in parts cost. Additionally, EHT has begun designing the inductive adder transformer.

For more information: http://www.eagleharbortech.com/

Acknowledgment

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